



Lista proiecte (Master, Diploma, R&D) 2009 - 2010

Nr.	Status	Type	General Fields	Project Title	Project Team	Project Management	
1	Taken	R&D/ Master	[Software IDE] [Embedded systems] [Real-time systems]	INVERTA: INtegrated Visual Environment for Real-Time Application Development	2 Students: > Dan RESTINEC (1 Master SE) > Olivia DATCU (1 Master SE)	Mihai MICEA	
				Project description: Continues the implementation and the development of the INVERTA integrated visual environment for designing and analyzing real-time applications. INVERTA allows the building, specification and visual display of real-time applications, designed as a set of tasks of different types, each task having a characteristic set of parameters (including parameters of time) and a set of control links with other tasks of the application.	Observatii: R&D Grants "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/) si OPEN-HARTS (http://dsplabs.cs.upt.ro/grants/openharts/). Descriere proiect Continuarea si dezvoltarea implementarii mediului vizual integrat INVERTA, destinat proiectarii si analizei aplicatiilor timp-real. INVERTA permite construirea, specificarea si afisarea vizuala a unei aplicatii timp-real, conceputa ca set de task-uri de diferite tipuri, fiecare task avand cate un set caracteristic de parametri (inclusiv parametri de timp) si un set de legaturi de control cu celelalte task-uri ale aplicatiei.	Observatii: R&D Grants "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/) si OPEN-HARTS (http://dsplabs.cs.upt.ro/grants/openharts/). Descriere proiect Continuation and implementation of a development tool plug-in for the INVERTA environment for WCET analysis for real-time applications tasks written on platforms of type ARM7 TDMI-S.	Observatii: R&D Grants "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/) si OPEN-HARTS (http://dsplabs.cs.upt.ro/grants/openharts/). Descriere proiect Continuarea si dezvoltarea implementarii unui utilitar de tip plug-in pentru mediu INVERTA, destinat analizei timpului WCET pentru task-urile aplicatiilor timp-real scrise pe platforme tip ARM7 TDMI-S.
2	Taken	R&D/ Diploma/ Master	[Software engineering] [Code analysis] [Compiling techniques] [Real-time systems]	Tool for the WCET analysis of real-time applications written in assembly (for the ARM) and C languages	2 Students: > Maximilien HAYOT (1 Master, ISEN-Lille) > Baptiste FRUILLUX (1 Master, ISEN-Lille)	Mihai MICEA	



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3	Taken	R&D	[Operating systems] [Real-time systems] [Embedded systems]	Porting, installing and configuring a real-time or embedded operating system for ARM 7/9 platforms	2 Students: > Sorin SOARE (III CTI) > Catalin-Andrei BORA (I Master IT)	Mihai MICEA
		Project description:	Takes into account operating systems such as QNX (www.qnx.com) or uCLinux (www.uclinux.org) to be ported and installed on the motherboard module of the WIT (Wireless Intelligent Terminal) from the CORE-TX Platform.		Observations: R&D Grant "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/)	
		Descriere proiect	Se au in vedere sisteme de operare cum ar fi QNX (www.qnx.com) sau uCLinux (www.uclinux.org), pentru a fi portate si instalate pe motherboard-urile modulelor WIT (Wireless Intelligent Terminal) de pe platforma CORE-TX.		Observatii: R&D Grant "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/)	
4	Partially Taken	R&D/ Diploma	[Embedded systems] [Data acquisition systems] [Real-time systems]	Data acquisition module for the WIT (CORE-TX Wireless Intelligent Terminal)	2 Students: > Deian COSAS (IV CTI) >	Dan CHICIUDEAN, Mihai MICEA
		Project description:	The design, implementation and testing of data acquisition mode for WIT. The development of driver software for this module. It has to use analog-digital converter incorporated in the LPC2000 family of processors, and the eventual use of a Atxmega microcontroller family as a acquisition coprocessor.		Observations: R&D Grant "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/)	
		Project description:	Proiectarea, executarea si testarea a modului de achiziții de date pentru WIT. Punerea la punct a driverului soft pentru acest modul. Se are in vedere utilizarea convertorului analog-numeric incorporat in procesoarelor din familia LPC2000, precum si eventuala folosire a unui microcontroler din familia Atxmega pe post de coprocesor de achiziție.		Observations: R&D Grant "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/)	

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5	Taken	R&D/ Master	[Embedded Systems] [Digital Video/Image Acquisition and Processing]	Image acquisition module	2 Students: > Ildiko KALLO (1 Master CE) > Adrian OAIDA (1 CTT)	Dan CHICIUDEAN, Mihai MICEA
			Project description: Video surveillance module for the CORE-TX platform. Implementation of a hardware and software for image acquisition mode, using a CMOS OEM capture device. One possible direction could be to adapt an CmuCAM3 type open source module (http://www.cmucam.org/). Another option would be the use of dedicated modules with serial interface, which offers on-chip JPEG compression (disadvantage: data transmission speed is modest, 1-2 fps).	Observatii: R&D Grant "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/)		
6	Taken	R&D	[Access control systems] [Security systems]	Access control system based on fingerprint recognition	1 Student: > Adrian OAIDA (1 CTT)	Dan CHICIUDEAN, Valentin STANGACIU



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7	Free	Diploma	[Digital signal processing] [Lab workshops]	Laboratory workshops for the Digital Signal Processing course on the Analog Devices BLACKFIN DSP platforms	2 Students: > >	Dan CHICIUDEAN, Andrei STANCOVICI, Mihai V. MICEA
				Project description: Laboratory Implementation of such audio effects as loopback, echo sound, FIR filters, sonar, etc. Porting the existing workshops, from the Freescale DSP platform to the Analog Devices BF537.	Observatii:	Observatii:
				Descriere proiect Realizarea unor lucrari de laborator de tipul loopback audio, ecou audio, filtre FIR, sonar, etc. Portarea actualelor lucrari de laborator de pe platforma cu Freescale DSP56F801 pe Analog Devices BF537	Observatii: Realizarea unor lucrari de laborator de tipul loopback audio, ecou audio, filtre FIR, sonar, etc. Portarea actualelor lucrari de laborator de pe platforma cu Freescale DSP56F801 pe Analog Devices BF537	Observatii: R&D Grant "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/). Use of the ultrasound modules and the electronic compass for the robot alignment: http://www.youtube.com/watch?v=ADMgJhlZxt4
8	Taken	R&D/ Diploma	[Embedded systems] [Digital signal processing] [Wireless communication]	Mobile robot alignment based on ultrasound signals	2 Students: > Sanziana INDREICA (An III CTI) > Cosmin GRUIN (An III CTI)	Andrei STANCOVICI, Mihai V. MICEA
				Project description: The objective of the work is finding and implementing solutions to align a mobile robot. The chosen alignment method must be faster than the existing methods. Must find an optimal alignment algorithm based on an existing algorithm. Each robot is equipped with an OLIIMEX development module and a module of perception. The robot's microcontroller, LPC2294 with ARM7TDMI-S architecture is based on a high performance 32-bit RISC type registers. The role of the perception module is to transmit and to receive ultrasonic signals.	Observatii: R&D Grant "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/). Utilizarea modulelor ultrasunice si compas electronic pentru alinierea robotilor. http://www.youtube.com/watch?v=ADMgJhlZxt4	Observatii: Obiectivul lucrarui constituie gasirea si implementarea a unei solutii de aliniere a robotilor mobili. Metoda de aliniere aleasa trebuie sa fie mai rapida decat metoda existenta. Trebuie gasit un algoritm optim de aliniere pornind de la algoritmul deja existent. Fiecare robot este echipat cu un modul de dezvoltare OLIMEX si un modul de perceptie. Microcontrolerul robotului, LPC2294 cu arhitectura ARM7TDMI-S, este bazat pe o performanta ridicata avand registre pe 32 de biti de tip RISC. Rolulul modulului de perceptie este de a transmite si de a receptie semnale ultrasunice.



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9	Taken	R&D/ Diploma/ Master	[Embedded systems] [Real-time systems] [Wireless communication]	Synchronization in wireless sensor networks and robotic environments	2 Students: > Valentin IFTIME (I Master CE) > Sebastian BARZEIANU (I Master CE)	Andrei STANCOVICI, Mihai V. MICEA
Project description:		<p>The module contains two modules of perception and coordination. It is needed that the two perception modules are synchronized with the coordinator. Both coordinator and perception modules are equipped with wireless communication modules. The coordinator sends a message to both modules, for example: At 11: 05 minutes and 15 seconds - raising the logical pin PORT2.10. Using a logic analyzer, one will follow if the raising time of both logical processors is the same.</p> <p>Coordination module and perception modules have already been implemented. The coordinator can be any PC computer that is connected by the serial port with a XBEE communication module. A perception module contains an LPC2294 microcontroller with ARM7DMI-S architecture which is connected to a XBEE communication module.</p>				
Descriere proiect		<p>Sistemul contine un modul de coordonare si doua module de perceptie. Se urmareste ca cele doua module de perceptie sa fie sincronizate cu ajutorul coordonatorului. Atat coordonatorul cat si modulele de perceptie sunt echipate cu module de comunicare wireless. Coordonatorul trimite un mesaj catre ambele module, ca de exemplu: La ora 11, 5 min si 15 secunde - ridică nivelul logic al pinului PORT2.10. Cu ajutorul unui analizor logic se va urmări ca momentul ridicării nivelului logic in cazul ambelor procesoare sa coincida. Modulul de coordonare si modulele de perceptie au fost deja realizate practic. Coordonatorul poate fi orice calculator PC ce are conectat pe portul serial un modul de comunicare Xbee. Un modul de perceptie contine un microcontroler LPC2294 cu arhitectura ARM7DMI-S la care este conectat un modul de comunicare Xbee.</p>				



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1.0	Taken	R&D	[Real-time systems] [Communication protocols] [Fieldbus systems]	Multi-Slave FTDMA (Flexible Time Division Multiple Access) Implementation of the PARSECS communication system for the WIT	1 Student: > Victor ADASCALTEI (An I CTI)	Gabriel N. CARSTOIU, Lucian UNGUREAN, Mihai V. MICEA
Project description:						Observations:
PARSECS (Predictable ARchitecture for Sensor Communication Systems) is a real-time communication architecture designed for modular smart sensors, particular for the WIT intelligent node. The current implementation allows full-duplex communication between a Master board (MotherBoard) and a Slave board (PMBoard). The project aims to interconnect multiple boards within the WIT with the support of the underlying SPI physical interface. Also, the full timeslot paradigm should be implemented and tested. Platform: a WIT prototype exists, consisting of 2 interconnected boards based on the LPC2294 microcontroller (Olimex LPC-H2294 eva-board). This will need to be extended to 3-4 boards. Available HW and SW tools: IDE and compiler (Keil uVision 3.x), debugger (ulINK2 debug tool), 32 channel logic analyzer (LA1032).						R&D Grant "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/).
Descriere proiect						Observatii:
PARSECS (Predictable ARchitecture for Sensor Communication Systems) is a real-time communication architecture designed for modular smart sensors, particular for the WIT intelligent node. The current implementation allows full-duplex communication between a Master board (MotherBoard) and a Slave board (PMBoard). The project aims to interconnect multiple boards within the WIT with the support of the underlying SPI physical interface. Also, the full timeslot paradigm should be implemented and tested. Platform: a WIT prototype exists, consisting of 2 interconnected boards based on the LPC2294 microcontroller (Olimex LPC-H2294 eva-board). This will need to be extended to 3-4 boards. Available HW and SW tools: IDE and compiler (Keil uVision 3.x), debugger (ulINK2 debug tool), 32 channel logic analyzer (LA1032).						R&D Grant "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/).



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1.1	Taken	R&D/ Diploma	[Real-time systems] [Battery powered/mobile devices] [Power management]	System Power Management implementation for the WIT based on advanced DPM techniques. Integrating DPM concepts in HARETICK	1 Student: > József SZILLAGYI (An III CTI)	Lucian UNGUREAN, Gabriel N. CARSTOIU, Mihai V. MIȚEA
Project description:				Observations: The WIT (Wireless Intelligent Terminal) prototype consists of several modules (boards), including the MotherBoard and the PMBoard. PMBoard handles the charge and discharge states of the WIT's power supply (rechargeable batteries). It also provides an array of power management parameters to the MotherBoard (current consumption for each module, battery voltage, temperature, estimated remaining operating time, etc.). Implementation of present algorithms in the field is expected (SPM and DPM), further improvements. The main idea of the project is to have the MotherBoard control and execute SPM algorithms based on data received from PMBoard and to model the various peripherals present on each module (board), at the DPM level. Platform: a WIT prototype exists, consisting of MotherBoard(LPC2294 microcontroller) and PMBoard (LPC2138). Available HW and SW tools: IDE and compiler (Keil uVision 3.x), debugger (uLINK2 debug tool), programmable power supplies (Hameg HM-7044).	R&D Grant "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/). Observatii: R&D Grant "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/).	
Descriere proiect				The WIT (Wireless Intelligent Terminal) prototype consists of several modules (boards), including the MotherBoard and the PMBoard. PMBoard handles the charge and discharge states of the WIT's power supply (rechargeable batteries). It also provides an array of power management parameters to the MotherBoard (current consumption for each module, battery voltage, temperature, estimated remaining operating time, etc.). Implementation of present algorithms in the field is expected (SPM and DPM), further improvements. The main idea of the project is to have the MotherBoard control and execute SPM algorithms based on data received from PMBoard and to model the various peripherals present on each module (board), at the DPM level. Platform: a WIT prototype exists, consisting of MotherBoard(LPC2294 microcontroller) and PMBoard (LPC2138). Available HW and SW tools: IDE and compiler (Keil uVision 3.x), debugger (uLINK2 debug tool), programmable power supplies (Hameg HM-7044).		

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12	Taken	R&D/ Master	[Real-time systems] [Operating systems]	Simulator for real-time task scheduling algorithms	2 Students: > Dan RESTITNEC (I Master SE) > Olivia DATCU (I Master SE)	Cristina STANGACIU, Mihai V. MICEA
				Project description: This is a real-time scheduler for the real-time tasks (tasks with time specifications) running on an embedded platform. This scheduler is currently under development. For this, the development of simulators and of a improved scheduler is required. The simulator will be done on computer in any programming language (C, C #, Java, etc.). There already is a initial version of the simulator, and the scheduler is already implemented on the platform, but it may accept improvements.	Observations: R&D Grants "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/) si OPEN-HARTS (http://dsplabs.cs.upt.ro/grants/openharts/). Descriere proiect Este vorba de un planificator pentru taskurile de timp real (taskuri cu specificatii de timp) ce ruleaza pe o platforma embedded. Acest planificator se afla in faza de dezvoltare. Pentru aceasta se doresc realizarea unor simuloare si imbunatatirea planificatorului. Simulatorul va fi realizat pe PC in orice limbaj de programare (C, C#, Java etc.). Se realizează o prima varianta de simulator, iar planificatorul este deja implementat pe platforma, dar acceptă imbunătățiri.	Observatii: R&D Grants "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/) si OPEN-HARTS (http://dsplabs.cs.upt.ro/grants/openharts/). Descriere proiect Este vorba de un planificator pentru taskurile de timp real (taskuri cu specificatii de timp) ce ruleaza pe o platforma embedded. Acest planificator se afla in faza de dezvoltare. Pentru aceasta se doresc realizarea unor simuloare si imbunatatirea planificatorului. Simulatorul va fi realizat pe PC in orice limbaj de programare (C, C#, Java etc.). Se realizează o prima varianta de simulator, iar planificatorul este deja implementat pe platforma, dar acceptă imbunătățiri.
13	Partially Taken	R&D/ Diploma	[Embedded systems] [Real-time systems] [Wireless communication]	Wireless networks routing protocol	2 Students: > Roxana NISTOR (IV CTI) >	Valentin STANGACIU, Mihai V. MICEA
				Project description: The project focuses on the development or adaptation of a wireless data routing protocol for the CORE-TX platform. The protocol must handle multi-layered network topologies and dynamic node attachment and detachment to the network. The wireless network is based on the ZigBee standard.	Observations: R&D Grant "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/). Descriere proiect Tema presupune realizarea sau adaptarea unui algoritm de rutare a informatiei, pentru platforma CORE-TX. Rutarea presupune direcționarea informației de la un nod emitor la un nod destinatie, acesta din urma nefind vizibil in mod direct de catre emitor. Este necesara si tratarea situatiei pierderii legaturii cu anumite noduri. Nodurile in discutie prezinta modalitati de comunicare wireless.	 R&D Grant "CORE-TX" (http://dsplabs.cs.upt.ro/grants/coretx/).

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14	Taken	Master	[Robotic collectives] [Emergent behavior] [Simulation tools]	eBMS - emergent Behavior Model Simulator	1 Student: > Madalina URSU (Master)	Razvan CIOARGA
						Observatii: R&D Grant "MELISSEVS" (http://dsplabs.cs.upt.ro/grants/melissevs/). Project description: Further development of the emergent behavior simulator, eBMS: - integration of the interpreter of the emergent behavior modeling language, eBML - integration of the communication simulator. Visual C, C# (.NET 2.0), XML, Socket, multi-thread.
						Observatii: R&D Grant "MELISSEVS" (http://dsplabs.cs.upt.ro/grants/melissevs/). Project description: Preluarea si dezvoltarea ulterioara a simulatorului de modelare a comportamentului emergent, eBMS: - integrarea interpretorului limbajului de modelare a comportamentului emergent, eBML; - integrarea simulatorului de comunicatie. Visual C, C# (.NET 2.0), XML, Socket, multi-thread.
15	Taken	Master	[Emergent behavior] [Web-based technologies] [Software engineering]	ERRIE - Emergent Behavior Based Web Crawler	1 Student: > Roxana URSU (Master)	Razvan CIOARGA
						Observatii: R&D Grant "MELISSEVS" (http://dsplabs.cs.upt.ro/grants/melissevs/). Project description: Further development of a emergent web crawler for the efficient collection and storage of Web sites.
						Observatii: R&D Grant "MELISSEVS" (http://dsplabs.cs.upt.ro/grants/melissevs/). Project description: Continuarea dezvoltarii unui web crawler emergent pentru colectarea si stocarea eficienta a site-urilor WEB.
16	Partially Taken	R&D/Diploma/ Master	[Robotic collectives] [Emergent behavior] [Robotic movement]	Emergent Movement in Collective Robotic Environments	2 Students: > Andrei BANC (1 Master IT)	Razvan CIOARGA
						Observatii: R&D Grant "MELISSEVS" (http://dsplabs.cs.upt.ro/grants/melissevs/). Project description: Further projects to study emerging movement of robots, using LEGO Mindstorms NXT kits.
						Observatii: R&D Grant "MELISSEVS" (http://dsplabs.cs.upt.ro/grants/melissevs/). Project description: Continuarea proiectelor pentru studiul miscarii emergente a robotilor, cu ajutorul kit-urilor LEGO Mindstorms NXT.
						Private info: banc.andrei@gmail.com



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<p>For further information or if you have any questions, please visit our website or contact us at the following addresses:</p>						
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