

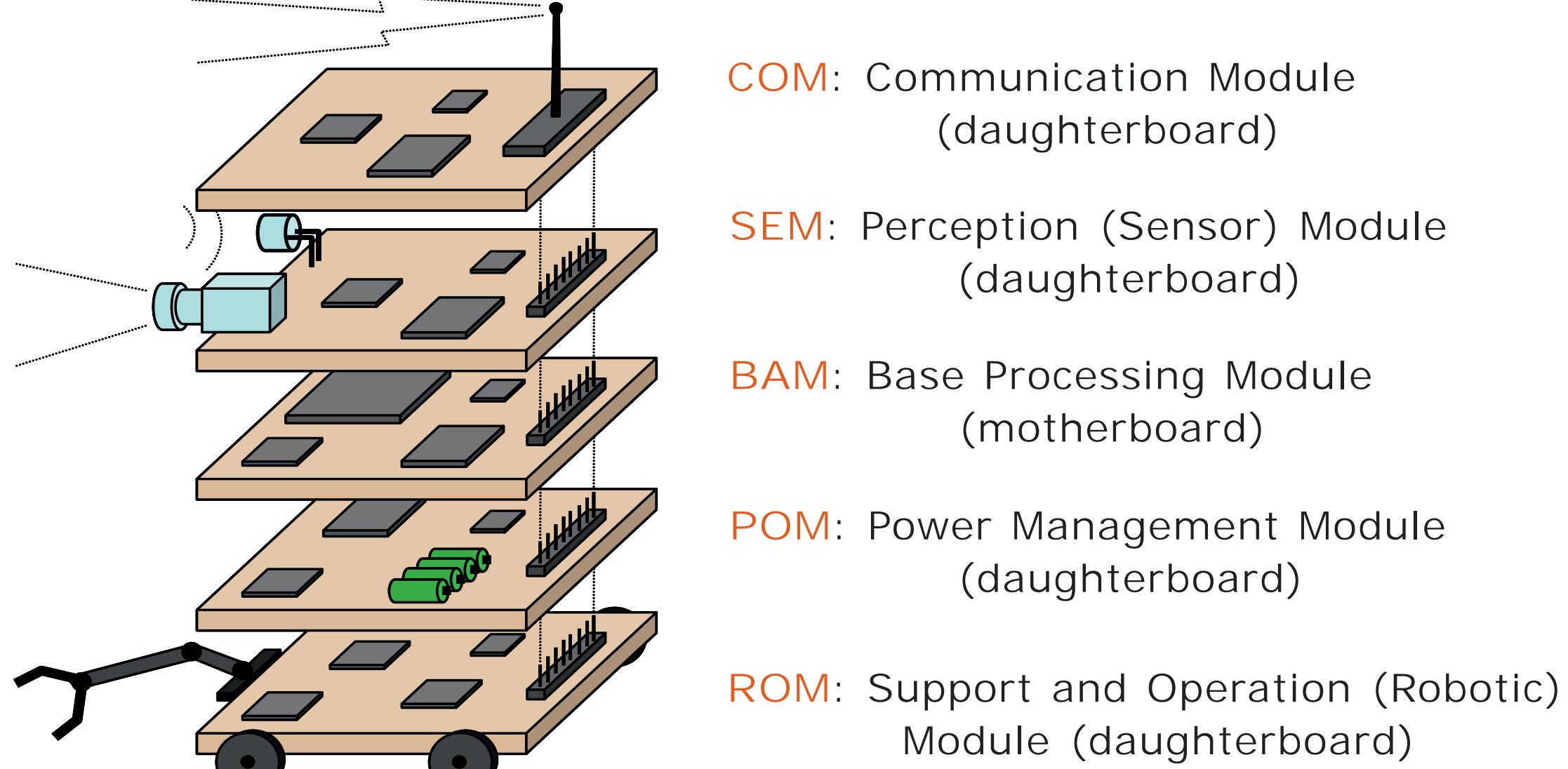
Collaborative Robotic Environment – the Timisoara eXperiment

Mihai V. MICEA, Vladimir I. CRETU, Dan CHICIUDEAN, Răzvan D. CIOARGĂ, Bogdan STRATULAT, Cristina STÂNGACIU, Valentin STÂNGACIU, Gabriel CÂRSTOIU, Lucian UNGUREAN, Andrei STANCOVICI

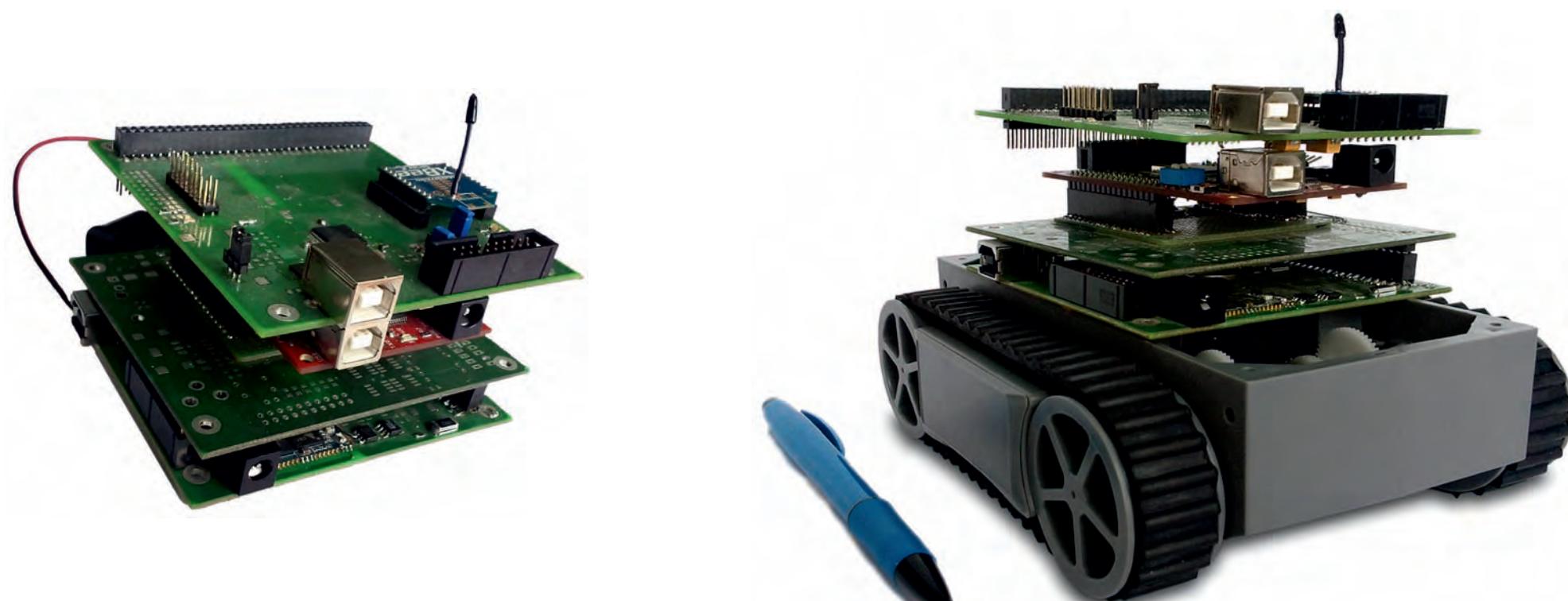
Overview

- ◆ Complex platform:
 - ▶ Studies on real-time autonomous microsystems with embedded intelligence
 - ▶ Applications of distributed artificial perception, intelligent sensor networks and collaborative robotic environments
- ◆ General architecture:
 - ▶ Perception and Operation Layer: set of autonomous microsystems with embedded intelligence (WITs)
 - ▶ Collaborative Communications Layer: based on the ZigBee wireless protocol
 - ▶ Background Control and Supervision Layer: central entity in charge of overall system configuration, control, data gathering and user interface (BRAIN)

General Architecture of the WIT



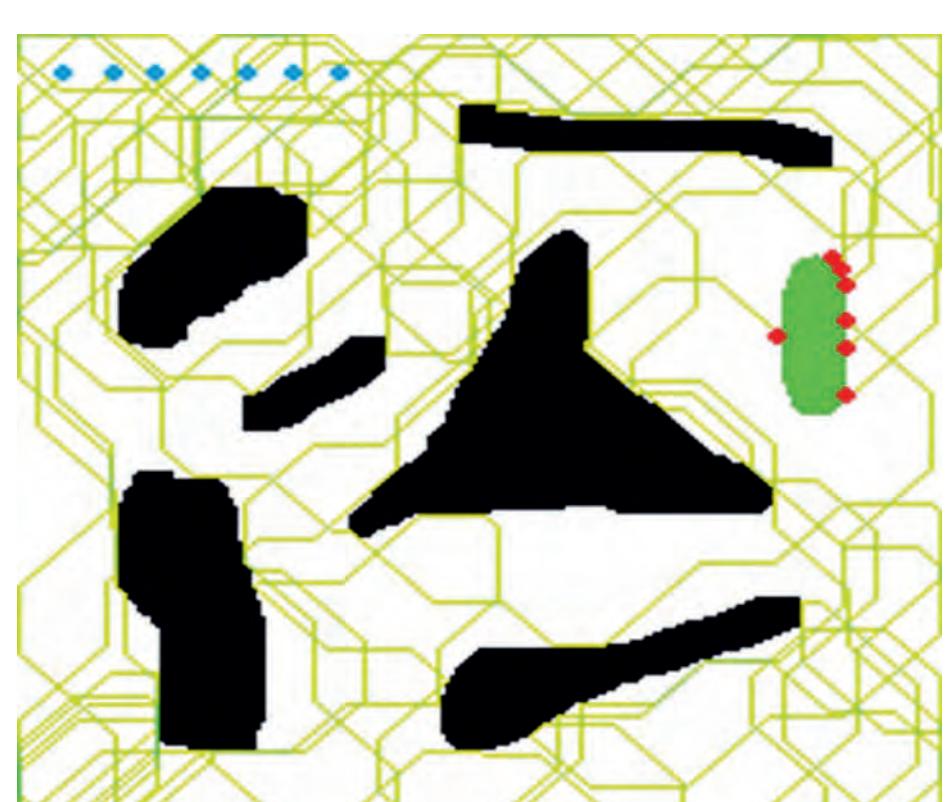
Prototype Versions of a Static WIT and a Mobile WIT



Background Control and Supervision: BRAIN

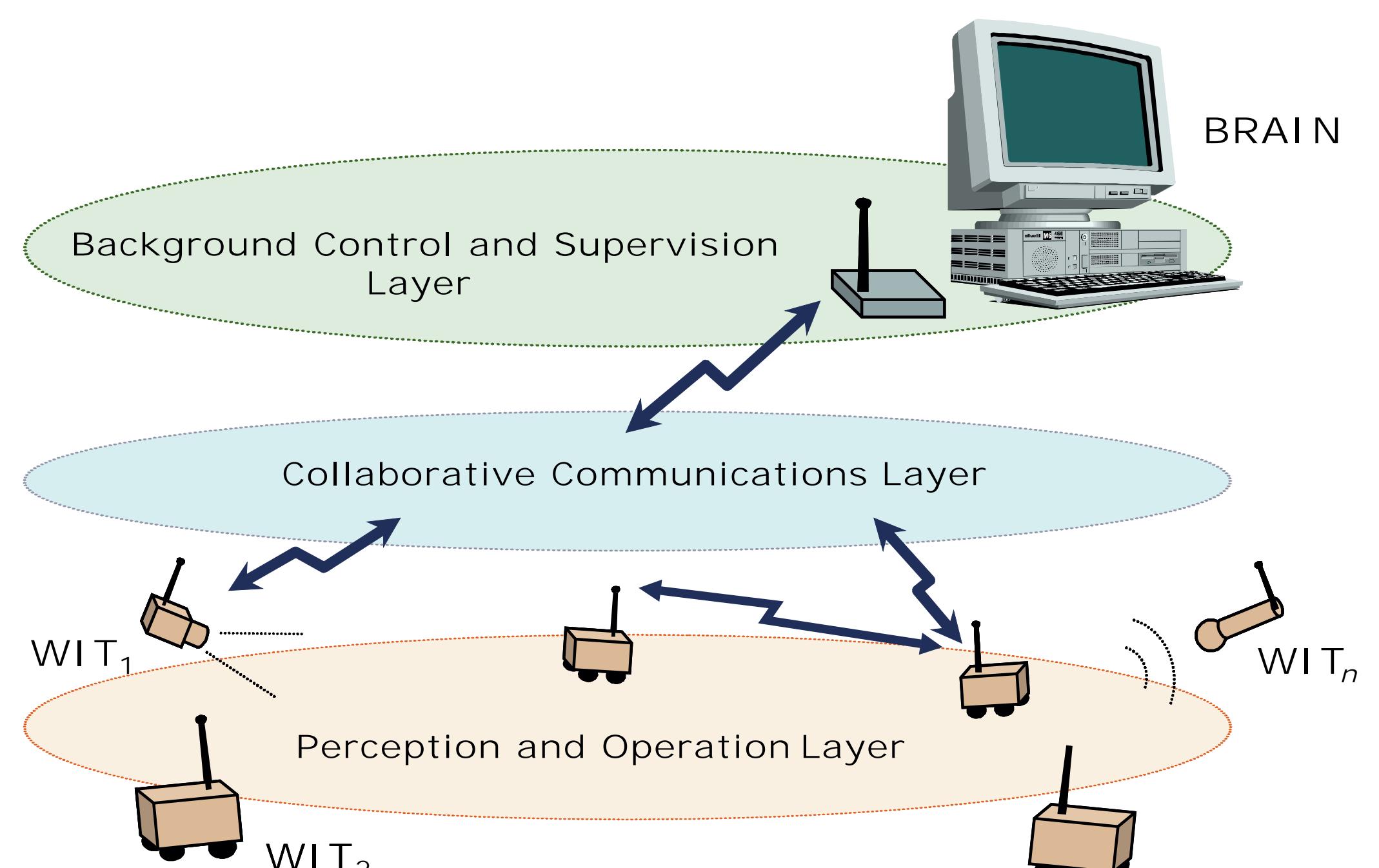
- ◆ BRAIN (Background Robotic Activity Induction Node):
 - ▶ Host computer with communication support
 - ▶ Reconfiguration/autoconfiguration of the collaborative environment
 - ▶ Development and analysis of behavior patterns
 - ▶ eBML - emergent Behavior Modeling Language
 - ▶ eBMS - emergent Behavior Modeling Simulator
 - ▶ General coordination → "background induction" techniques
 - ▶ Network data query, aggregation and analysis
 - ▶ Graphical user interface, configuration and status reports

eBMS Simulation of an Environment Exploration and Resource Gathering Application



- : Start point of mobile WIT
- : Resource
- : Finish point of mobile WIT
- : WIT movement trace
- : Obstacle

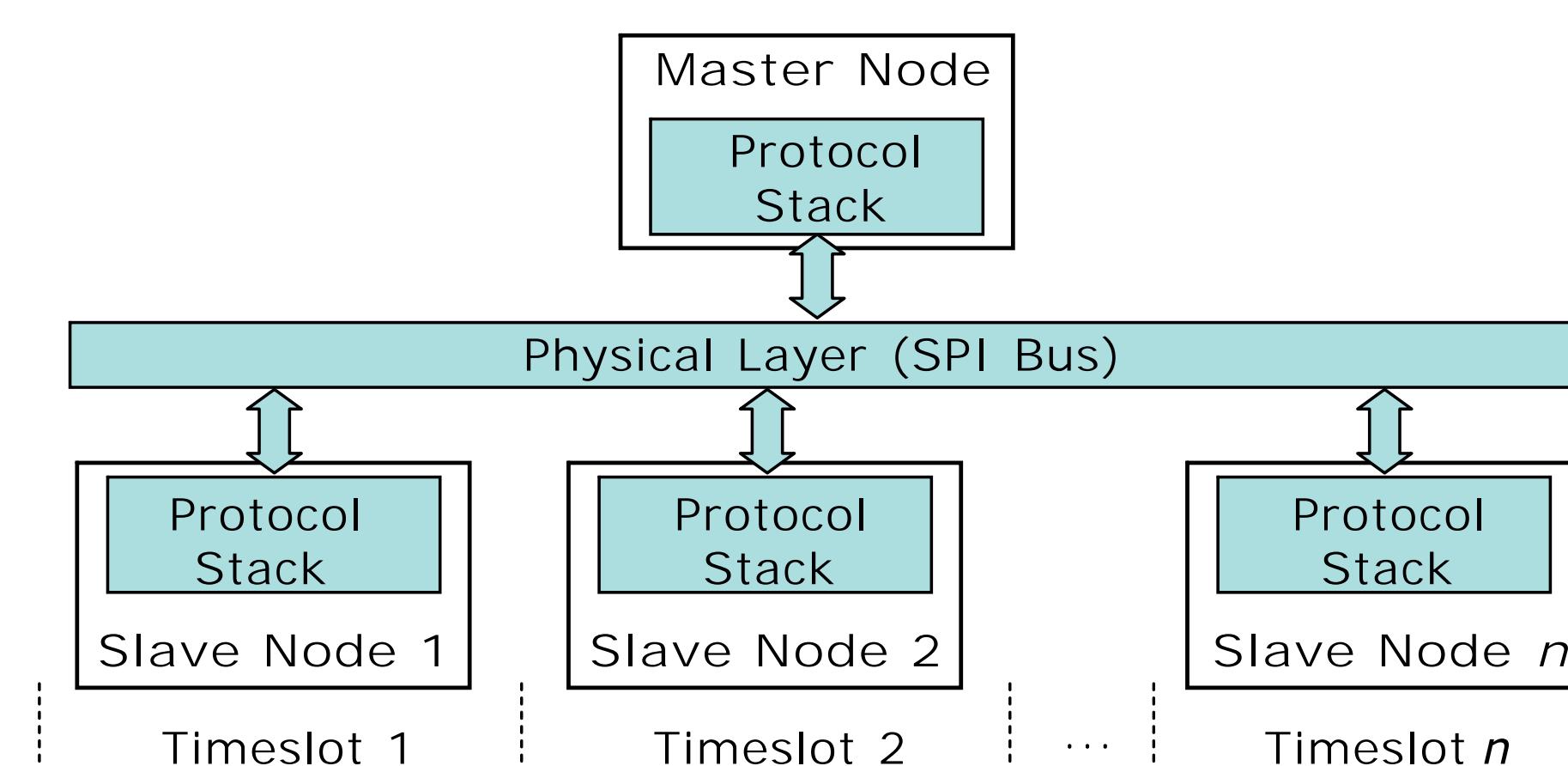
CORE-TX General Architecture



Perception and Operation: WIT

- ◆ WIT (Wireless Intelligent Terminal):
 - ▶ Perception (intelligent sensors) and/or operation (autonomous mini-robots)
 - ▶ Data communication capabilities (IEEE 802.15.4 "ZigBee" wireless protocol)
- ◆ General architecture:
 - ▶ Modular approach: 1 motherboard + up to 7 daughterboards
 - ▶ Board interconnection: PARSECS (Predictable Architecture for Sensor Communication Systems) → SPI bus in master-slave configuration
 - ▶ Base Processing Module, BAM (motherboard): central processing unit of the WIT; ARM9 based architecture; runs under the QNX® Neutrino® RTOS
 - ▶ Daughterboards: specialized functions (ROM, POM, SEM, COM); ARM7 based architecture; run under the HARETICK (Hard Real-Time Compact Kernel, <http://dsplabs.cs.upt.ro/grants/openharts/>) ⇒ highly predictable operation

PARSECS: Architecture and a Master-Slave Data Exchange Caption



Results

- ◆ 22+ papers published in scientific journals, periodicals and at conferences
- ◆ 1 major follow-up R&D grant (<http://dsplabs.cs.upt.ro/grants/melissevs/>)
- ◆ 3 operating WIT prototypes, in minimal architecture (BAM + POM + COM)
- ◆ Specifications of the eBML language and case study applications
- ◆ Prototype of the eBMS simulator and use case studies
- ◆ Studies and applications: wireless connectivity assessment and improvement; HARETICK kernel performance tests; BRAIN level data aggregation techniques